

ADC 6000 Series AXIe-based Digitizer Module



- High-speed waveform digitizer with built-in processing hardware and fast data transfer to external computer
- Up to **13 GHz** analog bandwidth of 8-bit A/D Converter with **40 GSPS** sampling rate in 1 channel mode
- **80 GSPS** sampling rate in interleaved mode. Requires two AXIe-based ADC 6131 modules and a signal splitter.
- **64 GBytes** of acquisition memory per module. Total of **896 GByte** of acquisition memory available in 14 slot AXIe chassis.
- Digital hardware-accelerated frequency response equalization, with custom programming capability
- FPGA-based reconfigurable digital signal processing with up to **7 GSPS** processing speed
- High-speed data transfer to host computer and graphic processors (GPU) for fast signal processing
- Up to 1.6 GByte/s data transfer rate to computer using PCI Express x4 Gen 2 link
- AXIe-based module 200 Watt maximum power consumption

Overview

ADC 6000 series AXIe-based Digital Acquisition and Processing Module combines high-speed waveform digitizer with built-in digital signal processing hardware, which enables mixed-domain signal capture and analysis with high-speed data transfer link to a computer. The ADC 6000 Module comes in a space-saving display-less 1U 19" AXIe module form factor.

The product addresses demanding ATE and OEM systems applications in semiconductors, military electronics, physics, astronomy, avionics, and a variety of other disciplines, as well as the disk drive head and media testing applications.

The waveform digitizer ADC 6000 series module features Agilent A/D converters with sampling rates up to 40 GSPS and analog bandwidth up to 13 GHz. ADC 6000 comes with up to 64 GBytes of acquisition memory that delivers the longest waveform capture time window available in a high bandwidth instrument.

ADC 6000 features an FPGA-based reconfigurable digital signal processor with up to 7 GSPS combined processing speed to convey massive time-critical computations directly inside the instrument.

The PCI Express Gen. 2 link provides fast transfer of the acquired data to the host computer's GPU and CPU-based processing back-end. The x4 link delivers 1.6 GByte/s sustained data transfer rate.

A Software Development Kit is supplied to control the instrument and to integrate ADC into existing AXIe measurement systems. Guzik also supplies Signal Display application for signal capturing and visualization.

The block diagram below shows the main components of ADC 6000 in an AXIe system in four-channel configuration:

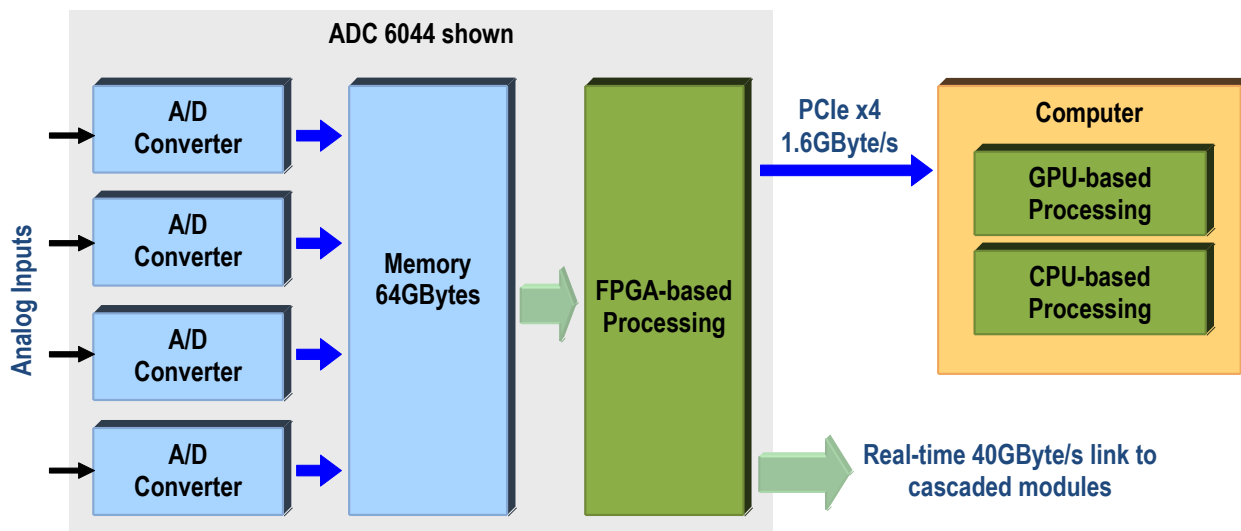


Figure 1. Block-diagram of four-channel ADC 6000 in standard Agilent AXIe chassis

Guzik AXIe-based Digitizer Modules

ADC 6000 Series includes four modules listed in the table below:

	ADC6131	ADC6082	ADC6044	ADC6083
Input Channels	1	2	4	3
Analog Bandwidth (-3db)	13 GHz	8 GHz	6.5 GHz (2-ch mode) 4 GHz (4-ch mode)	8 GHz (Ch-1) 4 GHz (Ch2 and Ch3)
Sampling Rate (per channel)	40 GSPS	20 GSPS	20 GSPS (2-ch mode) 10 GSPS (4-ch mode)	20 GSPS (Ch-1) 10 GSPS (Ch2 and Ch3)
Acquisition Memory (per channel)	8-64 GBytes ¹	4-32 GBytes	4-32 GBytes (2-ch mode) 2-16 GBytes (4-ch mode)	16 GBytes (Ch-1) 8 GBytes (Ch2 and Ch3)
PCI Express Interface to computer	x4 standard	x4 standard	x4 standard	x4 standard

Table 1. ADC 6000 Modules

Acquisition System

At the heart of the ADC 6000 Module are state of the art high-speed real-time analog to digital converter ASICs supplied by Agilent, which provide high speed waveform capture. The patented² digital hardware-accelerated frequency response equalization further improves the signal fidelity and effective number of bits.

At the maximum sampling rate of 40 GSamples/sec (25 psec per point), the ADC 6000 can capture up to 1.6 seconds of a real-time waveform into its ultra-long acquisition memory – up to 64 Gpoints for single channel configuration.

¹ Various memory size options are available

² U.S. Patent 7,408,495

Trigger

The ADC 6000 features a digital processing trigger. This feature makes use of the real-time hardware waveform processing capability and allows you to define trigger parameters based on the actual waveform data. Trigger on any input channel or one of two external trigger source inputs is provided. Trigger conditions are set using the ADC 6000 Signal Display software tool or from your application.

External Clock and I/O



The ADC 6000 features a 1 GHz external reference clock input, which can be used in place of the internal ADC clock.

Several test outputs are available for custom application support and system integration.

ADC 6000 provides a programmable calibrator output with a variety of test signals. You can connect this calibrator to any input channel and run an automatic calibration routine to ensure accurate operation of the instrument.

PCI Express Host Computer Interface

The ADC 6000 provides PCI Express Gen 2 x4 interface to the AXIe backplane. The PCI Express bridge card installs in the host computer, and a standard PCI Express x8 cable connects the AXIe chassis to the host computer. High speed waveform transfer with sustained data rates up to 1.6 GByte/sec is possible from this port back to the host computer.

With the upcoming AXIe-based Digital Processor DP 6000 Module, which provides four x8 PCIe Gen 2 interfaces to the host PC, the combined sustained data rate for data transfer from the ADC 6000 Module can be increased. This feature ensures that the standard x4 PCIe Gen 2 communication interface from the standard AXIe chassis to the computer will not become a bottleneck for your application.



Please refer to “AXIe ADC and DP configurations” document P/N 02-107561 for more details

Processing Overview and Capabilities

ADC 6000 provides various options for signal processing: FPGA, GPU, and CPU-based processing.

FPGA-based Processing

At the heart of the ADC 6000 are four industry-leading Altera Stratix™ IV FPGA's. These core processing elements combined with Guzik's implementation of customer-specified measurement algorithms provide end users with a truly tailored measurement solution where speed and throughput count. Once processed, results can be streamed via the ADC's PCI Express interface to a host computer at sustained data rates up to 1.6 Gbyte/sec.



The FPGA-based processor combined with Guzik's custom engineering capabilities provides you with the possibility to perform digital signal processing directly in ADC 6000 prior to sending waveform data out to computer. Many applications may require only processed results to be sent to the host computer rather than raw waveform data. Guzik will work directly with customers to implement custom processing capabilities drawing from years of experience in waveform analysis. Channel equalization, filtering, FFT, DFT, min/max, averaging, and parameter calculations among others are all available along with applications-specific requests. Guzik can provide custom services after a technical consultation regarding the specific application and required processing.

The combined FPGA processing resources are listed in the table below:

Processing Block	Number	Notes
Logic Cells	729,600	1 LUT and 1 flip-flop
Block RAM	4,940	9-Kbit blocks
	88	144-Kbit blocks
Multipliers	5,152	18-bit x 18-bit multipliers

Table 2. FPGA Resources in the expanded version of ADC 6000

GPU-based Processing

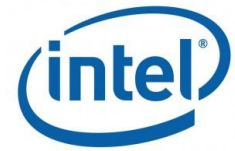


General-purpose computation on graphic hardware allows developers to reuse the computational algorithms available for GPU or develop their own algorithms on CUDA C or OpenCL. ADC 6000 is shipped with NVidia® GeForce GTX 570³ GPU. It is possible to use any NVidia® GPU with computing capability 2.0 or higher, if its power requirements are satisfied by the host computer power supply.

³ Current configuration. More powerful GPU cards may be shipped in the future

CPU-based Processing

In addition to FPGA-based and GPU-based computation, customers have an option to perform signal processing using a computer CPU. Multi-core processing libraries, such as OpenMP, allow utilizing full power of modern 12-core CPU computers. Once more powerful computers with more cores are released, you can upgrade your computer keeping your existing AXIe ADC 6000 Digitizer Module.

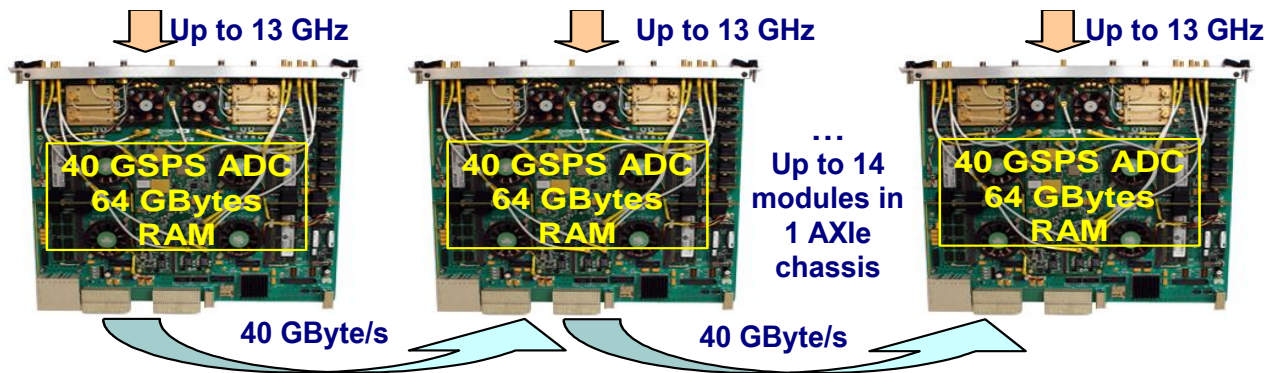


Ultra-fast GPU-based FFT Measurements

ADC 6000 performs frequency domain analysis using the Fast Fourier Transform (FFT) performed on GPU. Single NVIDIA® Tesla GPU card performs FFT calculations at a 2.5 GSPS processing speed. This means, for example, that if you collect data at 10 GSPS for 100 μ s, process in 400 μ s, you will get the full signal spectrum up to 5 GHz with resolution bandwidth 10 kHz – 500,000 spectral lines – in less than 0.5 ms.

Expandability

The ADC 6000 AXIe-based module, features a real-time 40GByte/s link through standard AXIe 62-pair Local Bus, which allows cascading multiple modules for increased memory, processing speed, and faster data streaming to computer. This is a special order configuration.



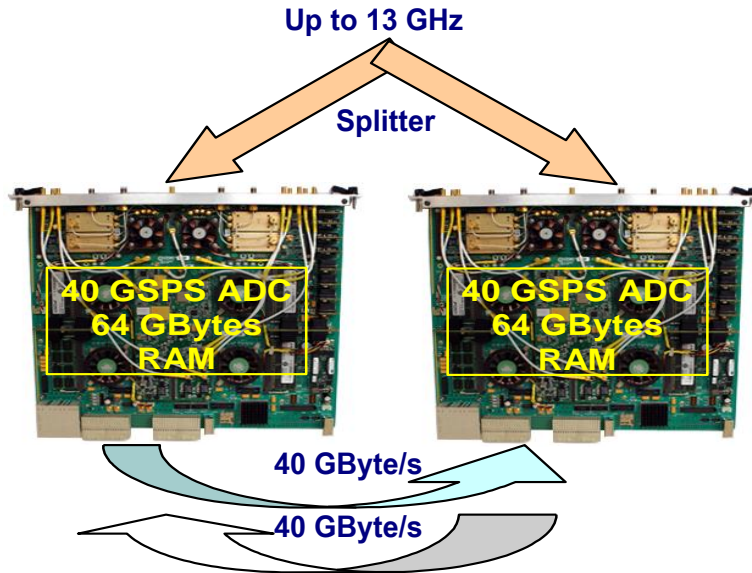
Up to 896 GBytes of memory is available for any channel in 14 slot AXIe chassis

Possible applications of the cascaded arrangement:

- Increased processing speed – acquire data by one board, transfer to and process by multiple boards, utilizing FPGA processors of several boards.
- Increased memory – acquire data by one board, transfer to multiple boards, utilizing memory of several boards. For example, combined memory of 14 boards is close to 1TByte.
- Increased sampling rate – acquire data by two or more boards and interleave them.
- Real-time data streaming – acquire data by one board, transfer to other boards, and stream to an array of PCs in real time.

Interleaving Modules

The ADC 6000 AXIe-based module's real-time 40GByte/s link through standard AXIe 62-pair Local Bus allows two 13GHz 40 GSPS ADC6131 Modules to be interleaved to achieve 80 GSPS sampling rate. The analog 13GHz signal is Split and connected to the two individual inputs of the ADC 6131 Modules.



Temperature Stabilization

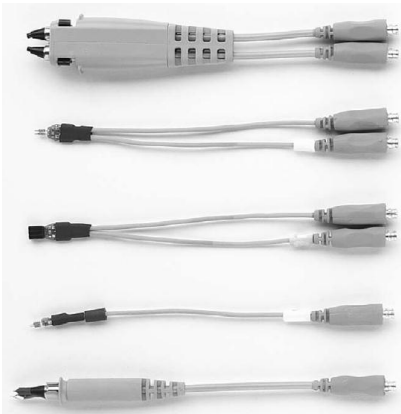
The ADC 6000 AXIe-based module keeps constant temperature for its critical A-to-D components. Tested at ambient temperatures from 14 C to 34 C in Guzik GSA 6000 stand-alone chassis.

ADC 6000 Module Designed for AXIe Standard

The AXIe ADC 6000 installs into an industry standard AXIe chassis together with other instruments, such as Agilent M8190A 12 GSPS Arbitrary Waveform Generator, and other AXIe modular instruments.



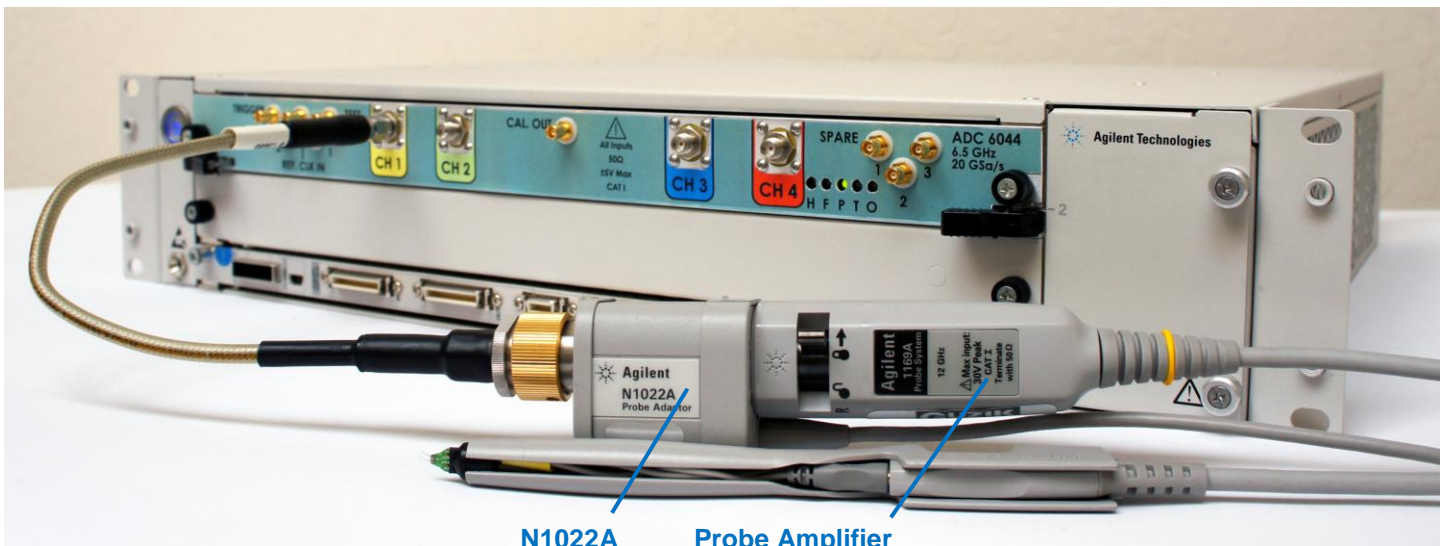
Signal Connection and Probing



For applications that require single ended or differential probing, Guzik recommends the **Agilent InfiniiMax** series of probing tools for use with the ADC 6000 AXIe-based Module. Detailed selection information can be found at the following link <http://cp.literature.agilent.com/litweb/pdf/5968-7141EN.pdf>. A wide variety of probe solutions up to 13 GHz in bandwidth can be purchased directly from Guzik.

The Agilent InfiniiMax Series⁴ features a variety of probe amplifier and body styles.

The interface to the ADC 6000's input connector is the Agilent N1022A Probe Adapter with an additional cable adapter pictured below.



The ADC 6000 Module features 50 ohm SMA connectors for inputs and MCX connectors for trigger and control I/O connections.

⁴ Agilent and InfiniiMax are registered trademarks of Agilent, Inc.

GSA Toolkit Software

To control the ADC 6000 AXIe-based Module Guzik provides a GSA Toolkit, which includes two software components:

1. GSA SDK – software development kit to create your custom standalone applications for ADC 6000 or to integrate ADC 6000 into your existing software environment; please refer to “*Guzik Signal Analyzer Software Development Kit User’s Guide*” document P/N 02-107544 for more details.
2. Signal Display application designed for easy instrument setup, waveform acquisition and visualization. Signal Display provides oscilloscope-like graphical user interface to display multiple signal waveforms, frequency spectrum, control acquisition parameters (sampling rate, duration, trigger settings, etc), and perform multiple trigger (multi-sector) acquisitions. The application allows for saving acquired signals to files for importing into EXCEL, MATLAB or other computational and analysis programs. You can load and display signals from files in various formats, including the previously saved waveforms. One of the useful features of Signal Display is tracking (monitoring) acquired signals during GSA SDK-based application execution. Please refer to “*Signal Display User’s Guide*” document P/N 02-107548 for more details.

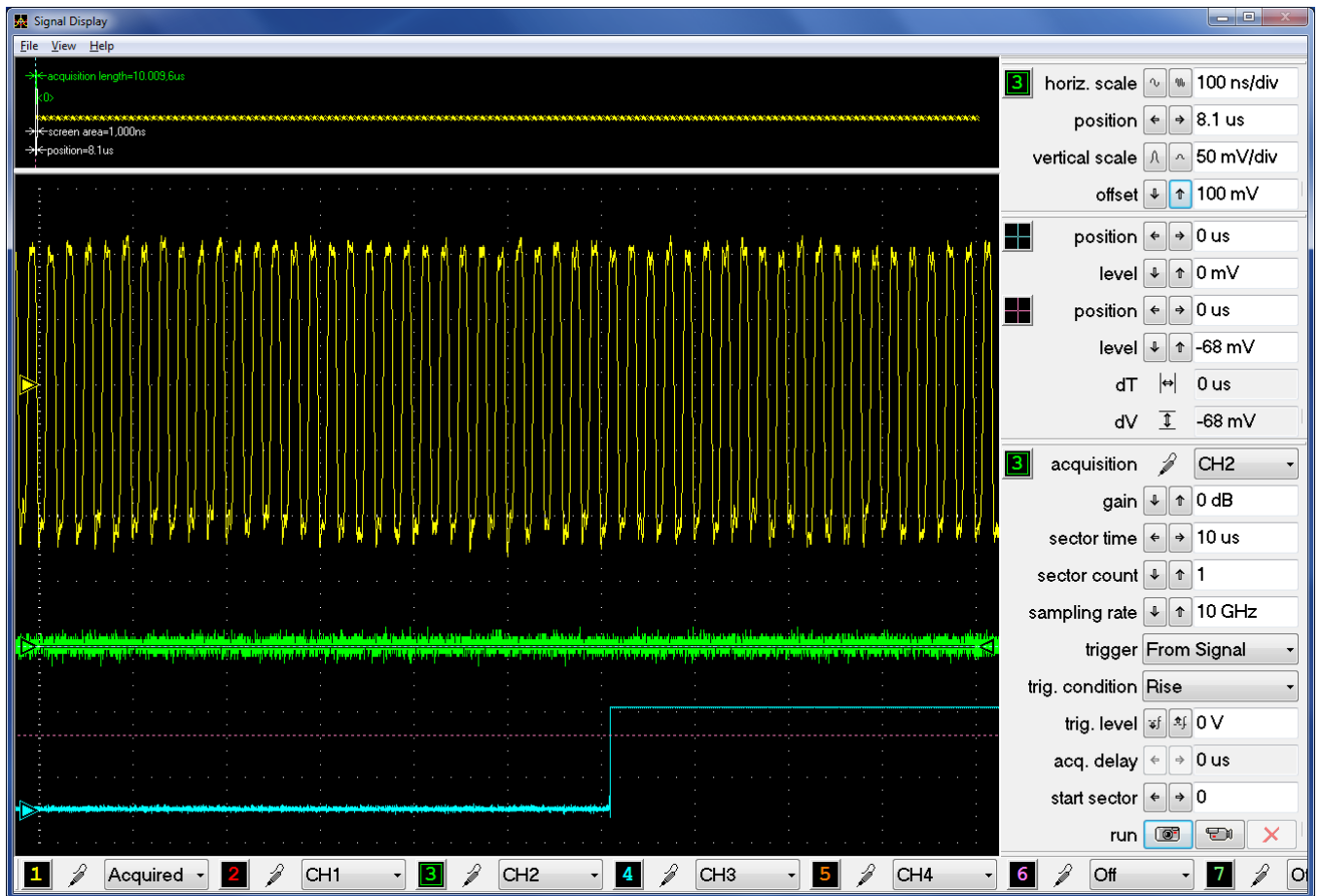


Figure 2. Signal Display Application

Specifications⁵

Vertical System ADC6083			Channel 1	Channel 2 and Channel 3	
Input Channels			1, SMA Female	1, SMA Female	2, SMA Female
Analog Bandwidth (-3db) ^{a,b}			8 GHz	6.5 GHz	4 GHz
Vertical Resolution			8 bits		
Input Impedance			50 ohm ± 3%		
Input Coupling			DC		
Maximum Input Voltage			± 5 V		
Input Sensitivity			40 mV .. 8 V (Full Scale) 1 mV/div .. 1 V/div (Scope UI) ^c		
Bandwidth Flatness ^{a,b} (-6 dBFs)			± 0.5 dB to 7 GHz -3 dB at 8 GHz	± 0.5 dB to 5 GHz -3 dB at 6.5 GHz	± 0.5 dB to 3.5 GHz -3 dB at 4 GHz
Effective Bits ^a (-3 dBFs, 50 mV/div)	Frequency				
	100 MHz		6.0	5.5	5.7
	1 GHz		5.9	5.4	5.7
	2 GHz		5.7	5.3	5.5
	3 GHz		5.6	4.7	5.5
	4 GHz		5.5	5.4	5.3
	6 GHz		5.1	5.2	–
	8 GHz		4.8		
Rise / Fall Time (10-90%)			49 ps	68 ps	104 ps
RMS Noise Floor ^a	Sensitivity (Full Scale)				
	Sensitivity (Scope UI)				
	40 mV	5 mV/div	315 uV	410 uV	241 uV
	80 mV	10 mV/div	400 uV	723 uV	426 uV
	160 mV	20 mV/div	580 uV	1.35 mV	817 uV
	400 mV	50 mV/div	1.60 mV	2.56 mV	1.86 mV
	800 mV	100 mV/div	3.10 mV	4.54 mV	3.67 mV
	1.6 V	200 mV/div	6.00 mV	13.1 mV	8.32 mV
4 V	500 mV/div	17.0 mV	24.3 mV	18.9 mV	
8 V	1 V/div	32.5 mV	45.5 mV	36.9 mV	

⁵ Specification values are typical. Specifications are subject to change.

Spurious Free Dynamic Range (SFDR) ^a (-3 dBFs, 50 mV/div)	<i>Frequency</i>			
	100 MHz	52 dBc	44 dBc	45 dBc
	1 GHz	52 dBc	46 dBc	47 dBc
	2 GHz	50 dBc	40 dBc	47 dBc
	3 GHz	52 dBc	33 dBc	47 dBc
	4 GHz	50 dBc	52 dBc	47 dBc
	6 GHz	45 dBc	42 dBc	–
8 GHz	40 dBc	–	–	
DC Gain Accuracy		± 2% of full scale at full resolution channel scale (± 2.5% for 5 mV/div)		
Offset Range	<i>Vertical Sensitivity</i>			
	0 ... 40 mV/div		± 0.4 V	
	40 ... 75 mV/div		± 0.9 V	
	75 ... 130 mV/div		± 1.6 V	
	130 ... 240 mV/div		± 3.0 V	
> 240 mV/div		± 4.0 V		
Offset Accuracy	<i>Offset Range</i>			
	< 3.5 V	± (2% of channel offset + 1% of full scale + 1 mV)		
	> 3.5 V	± (2% of channel offset + 1% of full scale)		
Dynamic range		± 4 div from center screen		
Channel to Channel Isolation (any two channels with equal V/div settings)	<i>Frequency</i>			
	< 2 GHz	48dB	55dB	55dB
	2 ... 4 GHz	48dB	45dB	45dB
	4 ... 6 GHz	48dB	36dB	–
	< 8 GHz	48dB	–	–
Return Loss		< -14 dB to 8 GHz	< -12 dB to 6 GHz	< -12 dB to 4 GHz
Acquisition System ADC6083				
Maximum Real Time Sample Rate		20 GSps	20 GSps	10 GSps
Memory Depth per Channel		16 Gpoints	16 Gpoints	8 Gpoints
(with optional larger memory)		(32 Gpoints)	(32 Gpoints)	(16 Gpoints)
Maximum Acquired Time per Channel at Highest Real Time Sample Rate		800 ms (1.6 s with optional larger memory)		

Vertical System GSA6044

2 Channel Mode

4 Channel Mode

Input Channels			2, SMA Female	4, SMA Female
Analog Bandwidth (-3db) ^{a,b}			6.5 GHz	4 GHz
Vertical Resolution			8 bits	
Input Impedance			50 ohm \pm 3%	
Input Coupling			DC	
Maximum Input Voltage			\pm 5 V	
Input Sensitivity			40 mV .. 8 V (<i>Full Scale</i>) 1 mV/div .. 1 V/div (<i>Scope UI</i>) ^c	
Bandwidth Flatness ^{a,b} (-6 dBFs)			\pm 0.5 dB to 5 GHz -3 dB at 6.5 GHz	\pm 0.5 dB to 3.5 GHz -3 dB at 4 GHz
Effective Bits ^a (-3 dBFs, 50 mV/div)	<i>Frequency</i>			
	100 MHz		5.5	5.7
	1 GHz		5.4	5.7
	2 GHz		5.3	5.5
	3 GHz		4.7	5.5
	4 GHz		5.4	5.3
	6 GHz		5.2	–
Rise / Fall Time (10-90%)			68 ps	104 ps
RMS Noise Floor ^a	<i>Sensitivity</i> (<i>Full Scale</i>)	<i>Sensitivity</i> (<i>Scope UI</i>)		
	40 mV	5 mV/div	410 μ V	241 μ V
	80 mV	10 mV/div	723 μ V	426 μ V
	160 mV	20 mV/div	1.35 mV	817 μ V
	400 mV	50 mV/div	2.56 mV	1.86 mV
	800 mV	100 mV/div	4.54 mV	3.67 mV
	1.6 V	200 mV/div	13.1 mV	8.32 mV
	4 V	500 mV/div	24.3 mV	18.9 mV
	8 V	1 V/div	45.5 mV	36.9 mV
Spurious Free Dynamic Range (SFDR) ^a (-3 dBFs, 50 mV/div)	<i>Frequency</i>			
	100 MHz		44 dBc	45 dBc
	1 GHz		46 dBc	47 dBc
	2 GHz		40 dBc	47 dBc
	3 GHz		33 dBc	47 dBc
	4 GHz		52 dBc	47 dBc
	6 GHz		42 dBc	–
DC Gain Accuracy			\pm 2% of full scale at full resolution channel scale (\pm 2.5% for 5 mV/div)	

Offset Range	<i>Vertical Sensitivity</i>		
	0 ... 40 mV/div		± 0.4 V
	40 ... 75 mV/div		± 0.9 V
	75 ... 130 mV/div		± 1.6 V
	130 ... 240 mV/div		± 3.0 V
	> 240 mV/div		± 4.0 V
Offset Accuracy	Offset Range		
	< 3.5 V	± (2% of channel offset + 1% of full scale + 1 mV)	
	> 3.5 V	± (2% of channel offset + 1% of full scale)	
Dynamic range	± 4 div from center screen		
Channel to Channel Isolation (any two channels with equal V/div settings)	<i>Frequency</i>		
	< 2 GHz	55dB	55dB
	2 ... 4 GHz	55dB	45dB
	4 ... 6 GHz	36	
Return Loss	< -12 dB to 4 GHz		< -12 dB to 6 GHz

Acquisition System ADC6044

Maximum Real Time Sample Rate	20 GSps	10 GSps
Memory Depth per Channel	16 Gpoints	8 Gpoints
(with optional larger memory)	(32 Gpoints)	(16 Gpoints)
Maximum Acquired Time per Channel at Highest Real Time Sample Rate	800 ms (1.6 s with 32G/16G option)	

Vertical System ADC6082

2 Channels

Input Channels	2, SMA Female		
Analog Bandwidth (-3db) ^{a,b}	8 GHz		
Vertical Resolution	8 bits		
Input Impedance	50 ohm \pm 3%		
Input Coupling	DC		
Maximum Input Voltage	\pm 5 V		
Input Sensitivity	40 mV .. 8 V (<i>Full Scale</i>) 1 mV/div .. 1 V/div (<i>Scope UI</i>) ^c		
Bandwidth Flatness ^{a,b} (-6 dBFs)	\pm 0.5 dB to 7 GHz -3 dB at 8 GHz		
Effective Bits ^a (-3 dBFs, 50 mV/div)	<i>Frequency</i>		
	100 MHz	6.0	
	1 GHz	5.9	
	2 GHz	5.7	
	3 GHz	5.6	
	4 GHz	5.5	
	6 GHz	5.1	
	8 GHz	4.8	
Rise / Fall Time (10-90%)	49 ps		
RMS Noise Floor ^a	<i>Sensitivity</i> (<i>Full Scale</i>)	<i>Sensitivity</i> (<i>Scope UI</i>)	
	40 mV	5 mV/div	315 uV
	80 mV	10 mV/div	400 uV
	160 mV	20 mV/div	580 uV
	400 mV	50 mV/div	1.60 mV
	800 mV	100 mV/div	3.10 mV
	1.6 V	200 mV/div	6.00 mV
	4 V	500 mV/div	17.0 mV
	8 V	1 V/div	32.5 mV
Spurious Free Dynamic Range (SFDR) ^a (-3 dBFs, 50 mV/div)	<i>Frequency</i>		
	100 MHz	52 dBc	
	1 GHz	52 dBc	
	2 GHz	50 dBc	
	3 GHz	52 dBc	
	4 GHz	50 dBc	
	6 GHz	45 dBc	
	8 GHz	40 dBc	
DC Gain Accuracy	\pm 2% of full scale at full resolution channel scale (\pm 2.5% for 5 mV/div)		

Offset Range	<i>Vertical Sensitivity</i>	
	0 to 40 mV/div	± 0.4 V
	40 to 75 mV/div	± 0.9 V
	75 to 130 mV/div	± 1.6 V
	130 to 240 mV/div	± 3.0 V
	> 240 mV/div	± 4.0 V
Offset Accuracy	Offset Range	
	< 3.5 V	± (2% of channel offset + 1% of full scale + 1 mV)
	> 3.5 V	± (2% of channel offset + 1% of full scale)
Dynamic range	± 4 div from center screen	
Channel to Channel Isolation (any two channels with equal V/div settings)	<i>Frequency</i>	
	< 8 GHz	48dB
Return Loss	< -14 dB to 8 GHz	

Acquisition System ADC6082

Maximum Real Time Sample Rate	20 GSps
Memory Depth per Channel	16 Gpoints (32 Gpoints is optional)
Maximum Acquired Time per Channel at Highest Real Time Sample Rate	800 ms (1.6 s with 32 Gpoints option)

Vertical System ADC6131

1 Channel

Input Channels	1, SMA Female	
Analog Bandwidth (-3db) ^{a,b}	13 GHz	
Vertical Resolution	8 bits	
Input Impedance	50 ohm \pm 3%	
Input Coupling	DC	
Maximum Input Voltage	\pm 5 V	
Input Sensitivity	40 mV .. 8 V (<i>Full Scale</i>) 1 mV/div .. 1 V/div (<i>Scope UI</i>) ^c	
Bandwidth Flatness ^{a,b} (-6 dBFs)	\pm 0.5 dB to 11 GHz -3 dB at 13 GHz	
Effective Bits ^a (-3 dBFs, 50 mV/div)	<i>Frequency</i>	
	100 MHz	5.6
	1 GHz	5.6
	2 GHz	5.5
	3 GHz	5.4
	4 GHz	5.2
	6 GHz	5.0
	8 GHz	4.6
	10 GHz	4.3
	13 GHz	4.2
Rise / Fall Time (10-90%)	32 ps	
RMS Noise Floor ^a	<i>Sensitivity</i> (<i>Full Scale</i>)	<i>Sensitivity</i> (<i>Scope UI</i>)
	40 mV	5 mV/div
	80 mV	10 mV/div
	160 mV	20 mV/div
	400 mV	50 mV/div
	800 mV	100 mV/div
	1.6 V	200 mV/div
	4 V	500 mV/div
	8 V	1 V/div
		485 uV
		550 uV
		670 uV
		2.10 mV
		3.80 mV
		7.40 mV
		21.6 mV
		45.8 mV
Spurious Free Dynamic Range (SFDR) ^a (-3 dBFs, 50 mV/div)	<i>Frequency</i>	
	100 MHz	52 dBc
	1 GHz	52 dBc
	2 GHz	52 dBc
	3 GHz	48 dBc
	4 GHz	45 dBc
	6 GHz	45 dBc
	8 GHz	42 dBc
	10 GHz	38 dBc

13 GHz

32 dBc

DC Gain Accuracy

± 2% of full scale at full resolution channel scale (± 2.5% for 5 mV/div)

Offset Range

Vertical Sensitivity

0 ... 40 mV/div	± 0.4 V
40 ... 75 mV/div	± 0.9 V
75 ... 130 mV/div	± 1.6 V
130 ... 240 mV/div	± 3.0 V
> 240 mV/div	± 4.0 V

Offset Accuracy

Offset Range

< 3.5 V	± (2% of channel offset + 1% of full scale + 1 mV)
> 3.5 V	± (2% of channel offset + 1% of full scale)

Dynamic range

± 4 div from center screen

**Channel to Channel Isolation
(any two channels with equal
V/div settings)**

N/A

Return Loss

< -12 dB to 12.5 GHz

Acquisition System ADC6131

Maximum Real Time Sample Rate

40 GSPS

Memory Depth per Channel

32 Gpoints (64 Gpoints is optional)

**Maximum Acquired Time per Channel at
Highest Real Time Sample Rate**

800 ms (1.6 s with 64Gpoints option)

Parametric Measurements Accuracy

TAA	± 2%
Pulse Width / Rise / Fall Time	± 3% or 20 ps whichever is greater
SNR	± 0.5 dB
Crest Factor	± 2%
Modulation	± 2%
Overwrite	± 0.2 dB

Trigger

Trigger Types	Internal edge trigger on an input channel External edge trigger
External Trigger Input	2, MCX Female
	Impedance 50 Ohm
	Voltage Range ± 5V
	Level Range ± 5V
	Max. Frequency 100 MHz

Control Signal Connections

Calibrator Output	1, MCX Female
	Impedance 50 Ohm
Optional External 10 MHz Reference Input (Configured instead of Spare)	1, MCX Female
	Level 0 to +10 dBm
	Impedance 50 Ohm
	Coupling AC
Optional External 50 MHz Reference Input (Configured instead of Spare)	1, SMA Female
	Level 0 to +10 dBm
	Impedance 50 Ohm
	Coupling AC
Optional External 50 MHz Reference Output (Configured instead of Spare)	1, SMA Female
	Level 800 mV p/p nominal
	Impedance 50 Ohm
	Coupling AC

External 1 GHz Clock Input		1, MCX Female
	Level Impedance Coupling	0 to +10 dBm 50 Ohm AC
Test Outputs		2, MCX Female
	Level	LV TTL

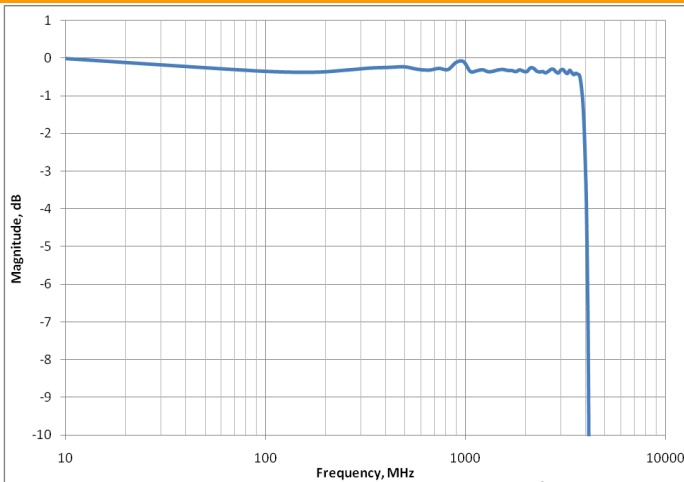
Host Computer

Transfer Interface	One x4 PCI-Express Generation 2 link via Guzik PCI-Express x8 switch card connected to the AXIe chassis
Transfer Speed	1.6 GBytes/s via x4 PCI-Express Generation 2 link
Operating System	32-bit Windows XP or Windows 7

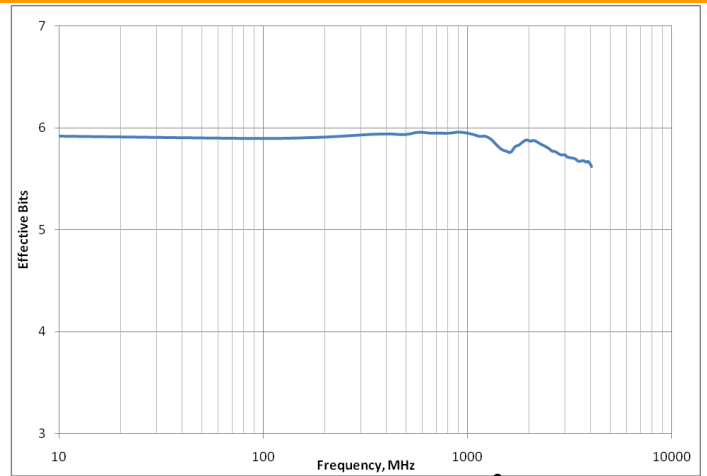
Module Physical

Weight	5.1 lbs / 2.3 kg
Power	200 Watt Max
Operating Temperature Range	+5 C to +40 C
Non-Operating Temperature	-40 C to +70 C
Operating Altitude	Up to 4,000 meters (12,000 feet)
Non-Operating Altitude	Up to 15,300 meters (50,000 feet)

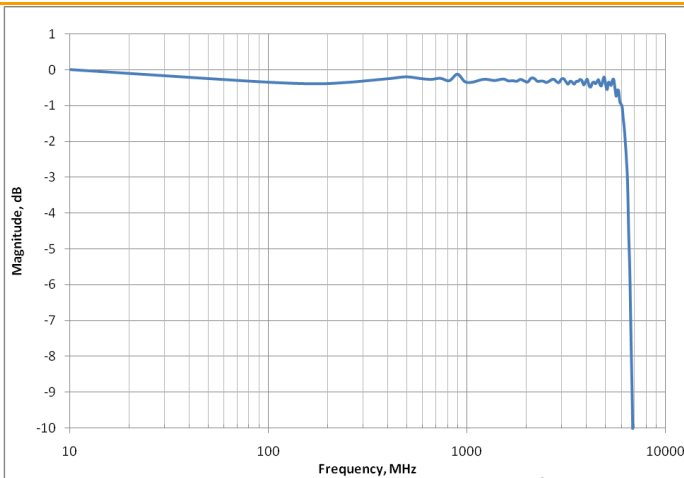
Performance Charts



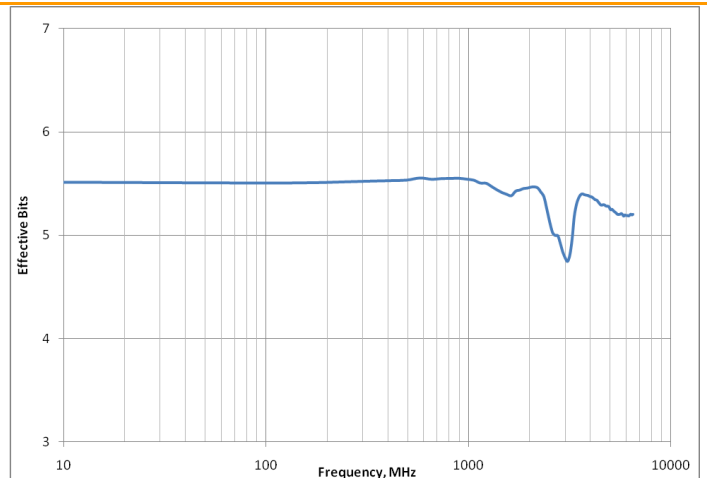
ADC6044 Frequency Response².
Sampling Rate 10 GS/Sec,
Analog Bandwidth 4 GHz.



ADC6044 Effective Bits².
Sampling Rate 10 GS/Sec,
Analog Bandwidth 4 GHz.



ADC6044 Frequency Response².
Sampling Rate 20 GS/Sec,
Analog Bandwidth 6.5 GHz.



ADC6044 Effective Bits².
Sampling Rate 20 GS/Sec,
Analog Bandwidth 6.5 GHz.

^a With digital equalization

^b 6-pole Butterworth approximation

^c Magnification is used below 5 mV/div. The major scale settings for Scope User Interface (UI) in Signal Display application are 5 mV/div, 10 mV/div, 20 mV/div, 50 mV/div, 100 mV/div, 200 mV/div, 500 mV/div, and 1 V/div. There are 8 vertical divisions on the screen.

Ordering and Availability

Base Module	P/N	Price	Lead Time
ADC 6000 AXIe-based Module with “basic” software	S90-620172-XX	Call	8-12 weeks
Options			
Multi-module Configuration		Call	Call
Accessories			
Guzik x8 PCIe Bridge Card to connect AXIe chassis to the host PC	S60-705574-XX	Call	Available
x8 PCIe 2 Meter Cable Assembly	S30-109656-XX	Call	Available

Software Packages

“Basic” software package includes:

- GSA SDK APIs: Acquisition, FFT, DFT
- Signal Display



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